Code No:A109210203 | R09 | SET-1

B.Tech II Year - I Semester Examinations, December 2011
ELECTRONIC DEVICES AND CIRCUITS
(COMMON TO EEE, ECE, CSE, EIE, BME, IT, MCT, E.COMP.E, ETM, ICE)
Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

1.a) What is Fermi level? By indicating the position of Fermi level in intrinsic, n-type and p- type semiconductor, explain its significance in semiconductors?

b) Sketch V-I characteristics of a PN diode for the following conditions:

i)	$R_f = 0$,	$V\gamma = 0$,	$R_r = \infty$
ii)	$R_f = 0$,	$V\gamma = 0.6V$,	$R_r = \infty$
iii)	$R_f =$ Non-zero, fixed value,	$V\gamma = 0$,	$R_r = \infty$
iv)	$R_f =$ Non-zero, fixed value,	$V\gamma = 0.6V$,	$R_r = \infty$

Where $V\gamma$ is the cut-in voltage, R_f is the forward dynamic resistance & R_r is the reverse dynamic resistance of the diode. [7+8]

2.a) Draw the block diagram of a regulated power supply and explain its operation.

b) A full wave bridge rectifier having load resistance of 100Ω is fed with 220V, 50Hz through a step-down transformer of turns ratio 11:1. Assuming the diodes ideal, find
i) DC output voltage
ii) Peak inverse voltage
iii) Rectifier efficiency. [9+6]

3.a) With a neat diagram explain the various current components in an NPN bipolar junction transistor & hence derive general equation for collector current, I_C?

b) What is Early-effect; explain why it is called as base-width modulation? Discuss its consequences in transistors in detail? [9+6]

4.a) What is 'Thermal Runaway' in transistors? Derive the condition to prevent 'Thermal Runaway' in Bipolar Junction Transistors.

b) A silicon NPN transistor has Ico = 20nA and β=150, V_{be} = 0.7V. It is operated in Common Emitter configuration (as shown in Figure.1) having Vbb = 4.5V,R_b= 150K,R_c = 3K, V_{cc} = 12V. Find the emitter, base and collector currents and also verify in which region does the transistor operate. What will happen if the value of the collector resistance is increased to very high values? [5+10]

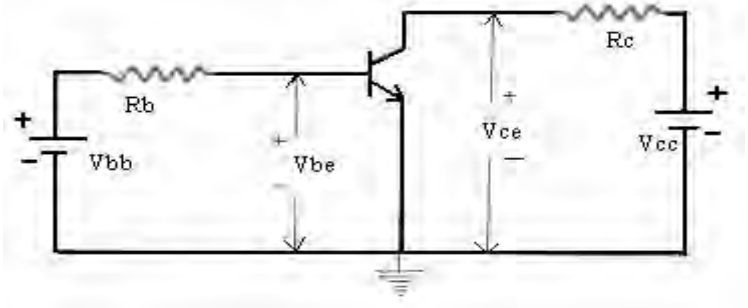

Figure.1

5.a) Draw the circuit diagram & small signal equivalent of CB amplifier using accurate h-parameter model. Derive expressions for A_V, A_I, R_i and R_0.

b) Draw small signal equivalent circuit of Emitter Follower using accurate h-parameter model. For the emitter follower circuit with R_S = 0.5K and R_L = 5K, calculate R_i, A_V and R_O. Assume, h_{fe} = 50, h_{ie} =1K, h_{oe} = 25 μA/V. [8+7]

6.a) Explain the construction & operation of a P-channel MOSFET in enhancement and depletion modes with the help of static drain characteristics and transfer characteristics?

b) "A depletion mode MOSFET can also be operated in enhancement mode but an enhancement mode MOSFET cannot be operated in depletion mode". Justify? [10+5]

7.a) Explain the need of biasing a Field Effect Transistor. With necessary equations and valid reasons explain why a simple 'fixed bias' arrangement for FETs is not used in practical applications?

b) A Common Source FET amplifier circuit shown in Figure.2 with un-bypassed R_S has the following circuit parameters: R_d = 15K, R_S = 0.5K, Rg = 1M, r_d = 5K, g_m= 5mS and V_{DD} = 20 V. Calculate A_V, A_I, R_i and R_0. [7+8]

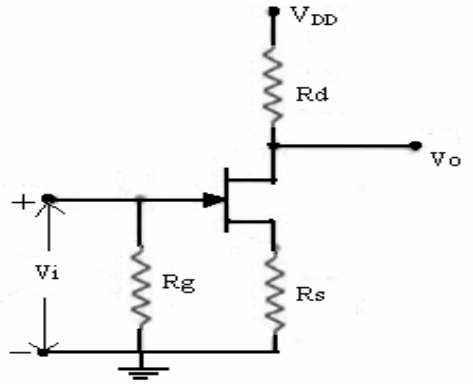

Figure.2

8.a) With neat energy band diagrams, explain the V-I characteristics of Tunnel diode. Also discuss the negative resistance property of tunnel diode.

b) With neat sketches explain the operation of Schottky Barrier Diode. [10+5]

****

Code No:A109210203 | R09 | SET-2

B.Tech II Year - I Semester Examinations, December 2011
ELECTRONIC DEVICES AND CIRCUITS
(COMMON TO EEE, ECE, CSE, EIE, BME, IT, MCT, E.COMP.E, ETM, ICE)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

1.a) What do you understand about the depletion region at a PN junction, with the help of necessary diagrams and derive expression for barrier potential.
b) Derive the expression for transition capacitance, C_T of a PN diode. [9+6]

2.a) With neat sketches explain the operation of a FWR with L- section filter & derive the expression for its ripple factor. Also explain the necessity of a bleeder resistor in a practical L- section filter.
b) Determine the ripple factor of an L-section filter comprising a 10H choke and 8μF capacitor, used with a FWR. The DC voltage at the load is 50V. Assume the line frequency as 50Hz. [10+5]

3.a) Draw the circuit diagram of NPN transistor in Common Emitter(CE) configuration. With neat sketches and necessary equations, describe its static input-output characteristics and clearly indicate the cut-off, saturation & active regions on the output characteristics?
b) Calculate the values of I_C and I_E for a transistor with α_{dc} = 0.99 and I_{CBO} = 5μA, if I_B is measured as 20 μA. [10+5]

4.a) What do you mean by biasing a transistor? Explain the need of biasing a transistor for the construction of a faithful amplifier?
b) Design a collector to base bias circuit using silicon transistor to achieve a stability factor of 20, with the following specifications: V_{CC} = 16V, V_{BE} = 0.7V, V_{CEQ} = 8V, I_{CQ} = 4 mA & β= 50. [7+8]

5.a) In the amplifier circuit shown in Figure.1, estimate input resistance and voltage gain? Also derive the expressions used?

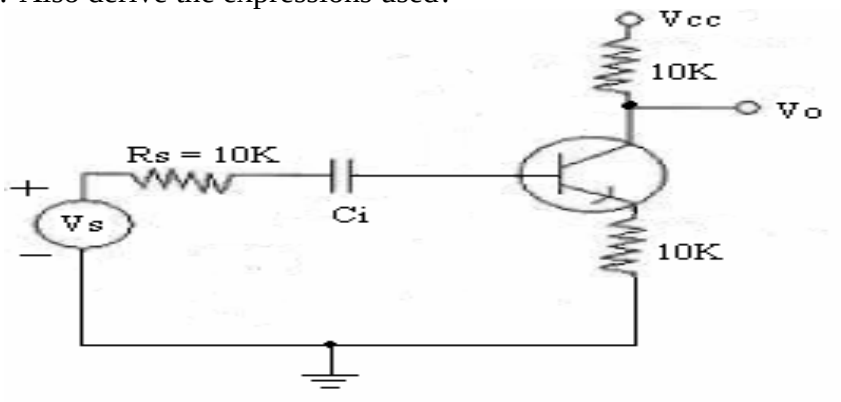

Figure.1

b) Compare CB, CE and CC amplifiers with respect to A_V, A_I, R_I & R_O? [10+5]

6.a) Explain the construction & operation of a P-channel MOSFET in enhancement and depletion modes with the help of static drain characteristics and transfer characteristics?

b) In an n-channel FET, the effective channel width is $3x\ 10^{-4}$cm and the donor impurity concentration is 10^{15} electrons/cm^3. Find the pinch-off voltage? [10+5]

7.a) Draw the basic circuit and small-signal model of Common Drain FET amplifier. Derive expressions for voltage gain and output resistance?

b) Compare the merits & demerits of a Bipolar Junction Transistor (BJT) with Field effect Transistor (FET) in detail? [8+7]

8.a) Draw the firing characteristics of SCR and briefly explain it.

b) Define the following with respect to SCR

i) Forward break over voltage

ii) Reverse break over voltage

iii) Holding current

iv) Gate trigger current. [7+8]

****

Code No:A109210203 | R09 | SET-3

B.Tech II Year - I Semester Examinations, December 2011
ELECTRONIC DEVICES AND CIRCUITS
(COMMON TO EEE, ECE, CSE, EIE, BME, IT, MCT, E.COMP.E, ETM, ICE)
Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

1.a) With the help of necessary sketches explain the potential distribution in an open circuited PN junction.
b) With the help of V-I Characteristics, explain the operation of a PN Diode under Forward bias and Reverse bias. [7+8]

2.a) With neat sketches explain the operation of a FWR with shunt capacitor filter & Derive the expression for its ripple factor.
b) A bridge rectifier uses four identical diodes having forward resistance of 5Ω each. Transformer secondary resistance is 5 ohms and the secondary voltage is 30V (rms). Determine the dc output voltage for I_{dc} = 200 mA and value of the output ripple voltage. [7+8]

3.a) Draw the circuit diagram of NPN transistor in Common Base (CB) configuration. With neat sketches and necessary equations, describe its static input- output characteristics and clearly indicate the cut-off, saturation & active regions on the output characteristics?
b) With reference to a BJT, define the following terms and explain:
i) Emitter efficiency.
ii) Base transportation factor.
iii) Large signal current gain. [9+6]

4.a) Obtain the condition for thermal stability of a BJT used in a biasing circuit?
b) Design a self bias circuit using silicon transistor to achieve a stability factor of 10, with the following specifications: V_{CC} = 16V, V_{BE} = 0.7V, V_{CEQ} = 8V, I_{CQ} = 4 mA & β= 50. [5+10]

5.a) Draw the circuit diagram & small signal equivalent circuit of CE amplifier using accurate h-parameter model. Derive expressions for A_V, A_I, R_i & R_0.
b) A bipolar junction transistor with h_{ie} = 1100Ω, h_{fe} = 50, h_{re} = $2.4x10^{-4}$, h_{oe} = 25 μA/V, is to drive a load of 1KΩ in Emitter-Follower arrangement. Estimate A_V, A_I, R_i & R_0? [8+7]

6.a) With the help of neat sketches and characteristic curves explain the construction & operation of a JFET and mark the regions of operation on the characteristics?
b) Show that in Field Effect Transistor, the transconductance, $g_m = g_{mo} [1- V_{GS}/ Vp]$ [8+7]

7.a) Draw the basic structure and equivalent circuit of UJT. Explain how the UJT can be used as a negative-resistance device with the aid of static characteristics**.**

b) In the common source FET amplifier shown in Figure.1, the transconductance and drain dynamic resistance of the FET are 5mA/V and 1MΩ respectively**.** Estimate A_V, R_i & R_0?

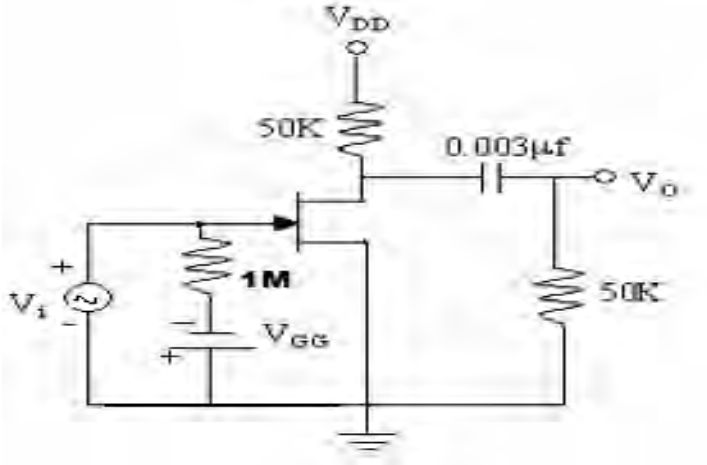

Figure.1

8.a) With neat sketches and necessary expressions describe V-I characteristics of a semiconductor photo diode?

b) With neat sketches and necessary expressions describe the operation of Varactor diode? [8+7]

****

Code No:A109210203 | R09 | SET-4

B.Tech II Year - I Semester Examinations, December 2011
ELECTRONIC DEVICES AND CIRCUITS
(COMMON TO EEE, ECE, CSE, EIE, BME, IT, MCT, E.COMP.E, ETM, ICE)
Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

1.a) Explain Avalanche and Zener break down mechanisms in semiconductors and compare them?

b) For the Zener diode circuit shown in Figure.1, determine V_L, V_R , I_Z & R. [5+10]

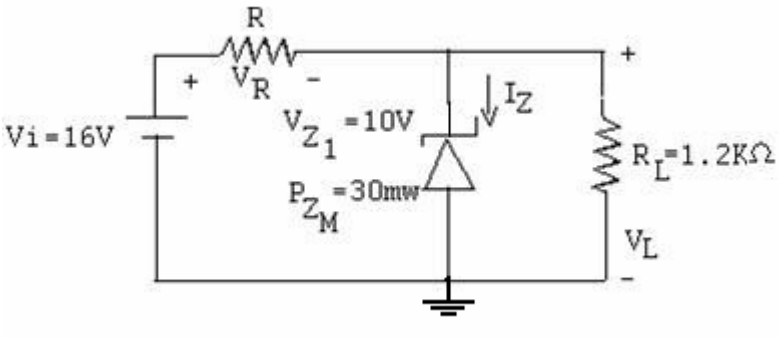

Figure.1

2.a) With reference to the Rectifiers, Explain the following terms:
i) Ripple Factor
ii) Efficiency
iii) Peak Inverse Voltage (PIV)
iv) % Regulation

b) A 230 V, 60Hz voltage is applied to the primary of a 5:1 step down, center tapped transformer used in a full wave rectifier having a load of 900Ω. If the diode resistance and the secondary coil resistance together have a resistance of 100 Ω, determine
i) DC voltage across the load.
ii) DC current flowing through the load.
iii) DC power delivered to the load.
iv) PIV across each diode. [8+7]

3.a) Draw the circuit diagram of NPN transistor in Common Collector (CC) configuration. With neat sketches and necessary equations, describe its static input- output characteristics and clearly indicate the cut-off, saturation & active regions on the output characteristics?

b) Derive the relationship among α, β and γ in transistors? [9+6]

4.a) What do you mean by biasing a transistor? Explain the need of biasing a transistor for the construction of a faithful amplifier?

b) Design an Emitter bias circuit using silicon transistor to achieve a stability factor of 20, with the following specifications: V_{CC} = 16V, V_{BE} = 0.7V, V_{CEQ} = 8V, I_{CQ} = 4 mA & β= 50. [7+8]

5.a) Draw the circuit and small-signal model of CE amplifier with unbypassed emitter resistor. Derive the expressions for input resistance & voltage gain?

b) A bipolar junction transistor with h_{ie} = 1100Ω, h_{fe} = 50, h_{re} = 2.4x10^{-4}, h_{oe} = 25 μA/V, is to drive a load of 1KΩ in CB amplifier arrangement. Estimate A_V, A_I, R_i & R_0. [8+7]

6.a) Explain the construction & operation of a N-channel MOSFET in enhancement and depletion modes with the help of static drain characteristics and transfer characteristics?

b) In an n-channel FET, the effective channel width is 3x 10^{-4}cm and the donor impurity concentration is 10^{15} electrons/cm^3. Find the pinch-off voltage? [10+5]

7.a) Show the self-bias arrangement for a Field Effect Transistor. With necessary expressions describe the procedure of Q-point establishment and stabilization?

b) In the common source FET amplifier shown in Figure.2, the transconductance and drain dynamic resistance of the FET are 5mA/V and 1MΩ respectively**.** Estimate A_V, R_i & R_0. [8+7]

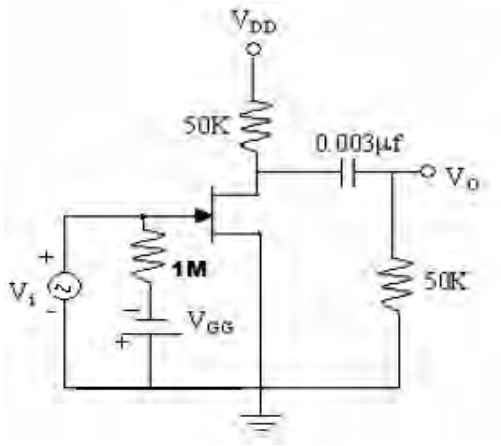

Figure.2

8.a) With neat energy band diagrams, explain the V-I characteristics of Tunnel diode. Also discuss the negative resistance property of tunnel diode.

b) Draw the two-transistor model of SCR and explain its operation. [10+5]

****

www.jntuworld.com || www.android.jntuworld.com || www.jwjobs.net || www.android.jwjobs.net

R09

Code No: 09A30306

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year I Semester Examinations, May/June-2013
Metallurgy and Material Science
(Common to ME, MCT, MIM, AME)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) Describe and illustrate the solidification process of a pure metal.
b) How does grain size influence the mechanical properties of materials? Describe any two methods of determination of grain size. [15]

2.a) What are the different solid solutions? Give examples.
b) Discuss about the various types of electron compounds. [15]

3.a) Differentiate between the following:
i) Eutectic and eutectoid transformation
ii) Peritectic and peritectoid.
b) What is Gibb's phase rule? Explain its importance. [15]

4.a) What are the advantages of steels over cast irons?
b) List out the properties and applications of grey cast iron.
c) What are the properties and applications of tool steels? [15]

5.a) Indicate the temperature range of the following heat treatments on Fe – Fe_3C equilibrium diagram (i) Annealing (ii) Normalizing (iii) Hardening (iv) Tempering.
b) Distinguish between Induction Hardening and Flame hardening. [15]

6. Describe the structure and properties of
a) Duraluminium
b) (α +β)Ti alloys
c) Aluminium bronzes
d) Muntz metal. [15]

7.a) Define ceramics. Classify them. Give some important applications of ceramics.
b) Discuss about any two abrasive materials. [15]

8. Write short notes on the following:
a) Metal matrix composites
b) Nano materials
c) Cryogenic treatment. [15]

---oo0oo---

JNTUWORLD.COM

www.jntuworld.com || www.jwjobs.net

www.jntuworld.com www.jwjobs.net

Code No:A109210203 | R09 | SET-1

B.Tech II Year I Semester Examinations, May-June, 2012
ELECTRONIC DEVICES AND CIRCUITS
(COMMON TO BME, CSE, EEE, ECE, ECC, EIE, ETM, IT, ICE, MCT)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

\- - -

1.a) Explain the concept of diode capacitance. Derive expression for transition capacitance?
b) Find the value of D.C. resistance and A.C resistance of a Germanium junction diode at 25^0 C with reverse saturation current, I_o = 25μA and at an applied voltage of 0.2V across the diode. [8+7]

2. Define the following terms and derive the equations with respect to half-wave rectifier:
i) Ripple factor ii) Peak inverse voltage
iii) Rectification efficiency iv) % Regulation. [15]

3.a) With neat sketches and necessary waveforms, explain the input and output characteristics of a BJT in CB configuration. Also derive expression for output current.
b) Derive the relation among α, β and γ. [10+5]

4.a) Explain the basic requirements of transistor biasing. Verify these requirements in collector to base bias circuit.
b) Design a fixed bias circuit using silicon transistor, with the following specifications: V_{CC} = 16V, V_{BE} = 0.7V, V_{CEQ} = 8V, I_{CQ} = 4 mA & β= 50. [8+7]

5. Draw the circuit diagram, AC equivalent & small signal equivalent of Common Base amplifier using accurate h-parameter model. Derive expressions for A_{Vs}, A_{Is}, R_I & R_O. [15]

6.a) Explain the construction & operation of an N-channel enhancement and depletion MOSFET with the help of static drain characteristics and transfer characteristics.
b) Define pinch-off voltage and transconductance in field effect transistors. [12+3]

7.a) Draw the small-signal model of common drain FET amplifier. Derive expressions for voltage gain and output resistance.
b) Calculate voltage gain $A_V = V_O/V_i$ and R_O at 1KHz for the circuit shown in Figure.1. FET parameters are gm=2mA/V and rd =10k. Neglect capacitances. [8+7]

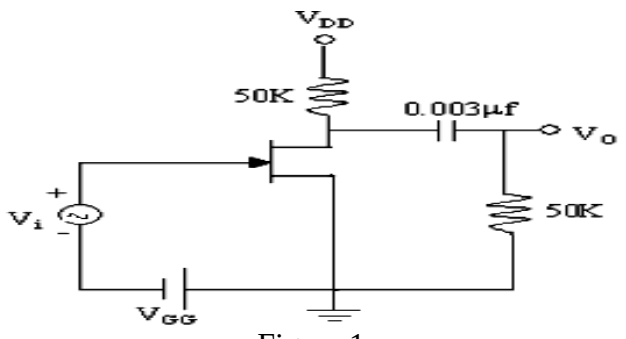

Figure.1

8. With neat energy band diagrams, explain the V-I characteristics of Tunnel diode in detail. Also explain the negative-resistance region in the characteristics and applications of Tunnel diode. [15]

****

www.jntuworld.com

www.jntuworld.com www.jwjobs.net

Code No:A109210203 | R09 | SET-2

B.Tech II Year - I Semester Examinations, May-June, 2012
ELECTRONIC DEVICES AND CIRCUITS
(COMMON TO BME, CSE, EEE, ECE, ECC, EIE, ETM, IT, ICE, MCT)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

\- - -

1.a) What do you understand by depletion region at p-n junction? What is the effect of forward and reverse biasing of p-n junction on the depletion region? Explain with necessary diagrams.
b) Explain Zener and avalanche breakdown mechanisms in detail. [8+7]

2.a) Draw the circuit diagram of full-wave rectifier with inductor filter. Explain its operation with necessary equations.
b) A HWR circuit supplies 100mA DC current to a 250Ω load. Find the DC output voltage, PIV rating of a diode and the r.m.s. voltage for the transformer supplying the rectifier. [8+7]

3.a) With neat sketches and necessary waveforms, explain the input and output characteristics of a BJT in CE configuration. Also derive expression for output current.
b) Calculate the collector current and emitter current for a transistor with $\alpha = 0.99$ and $I_{CBO} = 50\mu A$ when the base current is $20\mu A$. [10+5]

4.a) What is thermal runaway in transistors? Obtain the condition for thermal stability in transistors.
b) Design a self bias circuit using silicon transistor to achieve a stability factor of 10, with the following specifications: $V_{CC} = 16V$, $V_{BE} = 0.7V$, $V_{CEQ} = 8V$, $I_{CQ} = 4$ mA & $\beta = 50$. [6+9]

5. Draw the circuit diagram, AC equivalent & small signal equivalent of Emitter Follower amplifier using accurate h-parameter model. Derive expressions for A_{Vs}, A_{Is}, R_I & R_O. [15]

6.a) With the help of neat sketches and characteristic curves explain the construction & operation of a JFET and mark the regions of operation on the characteristics.
b) Derive expression for transconductance in a field effect transistor. [10+5]

7.a) Draw the small-signal model of common source FET amplifier. Derive expressions for voltage gain and output resistance.
b) Give the UJT symbol and simplified equivalent circuit with external resistors included. Describe its negative-resistance nature, with the help of V-I characteristics. [7+8]

8.a) With neat sketches, explain the principle of operation of Schottky Barrier Diode.
b) With neat sketches, explain V-I characteristics of semiconductor Photo Diode. [8+7]

****

JNTUWORLD

www.jntuworld.com

www.jntuworld.com www.jwjobs.net

Code No:A109210203 | R09 | SET-3

B.Tech II Year - I Semester Examinations, May-June, 2012
ELECTRONIC DEVICES AND CIRCUITS
(COMMON TO BME, CSE, EEE, ECE, ECC, EIE, ETM, IT, ICE, MCT)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

\- - -

1.a) Explain about various current components in a forward biased p-n junction diode.
b) With neat sketches and necessary waveforms explain about the regulation characteristics of Zener diode. [7+8]

2.a) Draw the circuit of full-wave rectifier with capacitor filter. Explain its operation with necessary equations.
b) A full wave rectifier circuit uses two silicon diodes with a forward resistance of 20Ω each. A DC voltmeter connected across the load of 1KΩ reads 55.4 volts. Calculate
i) I_{rms} ii) Average voltage across each diode
iii) ripple factor iv) Transformer secondary voltage rating. [7+8]

3.a) With neat sketches and necessary waveforms, explain the input and output characteristics of a BJT in CE configuration. Also derive expression for output current.
b) The reverse leakage current of the transistor when connected in CB configuration is 0.2 μA while it is 18 μA when the same transistor is connected in CE configuration. Calculate α and β of the transistor. [10+5]

4.a) Explain how I_{CO} variations are compensated with the help of diode and thermistor in transistor biasing circuits?
b) Design a collector to base bias circuit using silicon transistor to achieve a stability factor of 20, with the following specifications: V_{CC} = 16V, V_{BE} = 0.7V, V_{CEQ} = 8V, I_{CQ} = 4 mA & β= 50. [7+8]

5. Draw the basic circuit, ac equivalent and h-parameter model of a Common Emitter amplifier. Derive expressions for A_{Vs}, A_{Is}, R_I & R_O. [15]

6.a) Explain the construction & operation of an P-channel enhancement and depletion MOSFET with the help of static drain characteristics and transfer characteristics.
b) Explain why field effect transistor is called as unipolar and voltage controlled device. [12+3]

7.a) Draw the small-signal model of common gate FET amplifier. Derive expressions for voltage gain and input resistance.
b) A Common Source FET amplifier circuit shown in Figure.1 with unbypassed R_S has the following circuit parameters: R_d = 15K, R_S = 0.5K, Rg = 1M, r_d = 5K, g_m= 5mS and V_{DD} = 20 V. Calculate A_V & R_O. [8+7]

JNTUWORLD

www.jntuworld.com

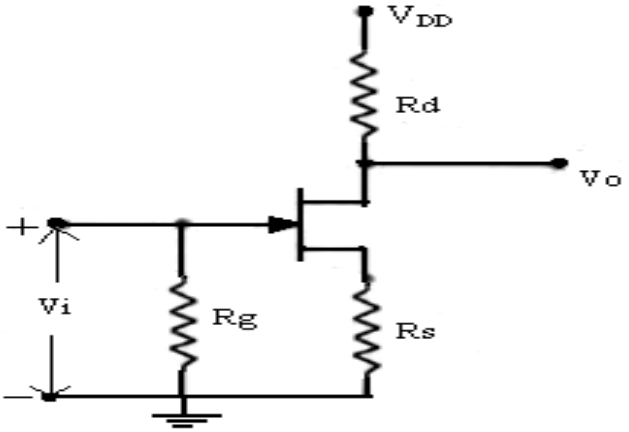

Figure.1

8. With neat energy band diagrams, explain the V-I characteristics of Tunnel diode in detail. Also explain the negative-resistance region in the characteristics. [15]

****

JNTUWORLD

www.jntuworld.com www.jwjobs.net

Code No:A109210203 | R09 | SET-4

B.Tech II Year - I Semester Examinations, May-June, 2012
ELECTRONIC DEVICES AND CIRCUITS
(COMMON TO BME, CSE, EEE, ECE, ECC, EIE, ETM, IT, ICE, MCT)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

- - -

1.a) With neat sketches and necessary waveforms explain the volt ampere characteristics of PN diode.
b) Explain the temperature dependence of VI characteristics of PN diode.
c) Compare ideal and practical diodes. [8+4+3]

2.a) Draw the circuit of full-wave rectifier with L-section filter and derive expression for its ripple factor.
b) A 230 V, 60Hz voltage is applied to the primary of a 5:1 step down, center tapped transformer used in a full wave rectifier having a load of 900Ω .If the diode resistance and the secondary coil resistance together has a resistance of 100Ω, determine
i) dc voltage across the load. ii) dc current flowing through the load.
iii) dc power delivered to the load. iv) PIV across each diode. [7+8]

3.a) With the help of a neat diagram explain different current components in an NPN bipolar junction transistor.
b) With reference to bipolar junction transistors, define the following terms and explain.
i) Emitter efficiency.
ii) Base Transportation factor.
iii) Large signal current gain. [9+6]

4.a) Explain the basic requirements of transistor biasing. Verify these requirements in Emitter feedback bias circuit.
b) An NPN Silicon transistor with β=50 is used in a common emitter circuit with V_{CC}=10V, R_C=2K. The bias is obtained by connecting a 100K resistance from collector to base. Find
i) Q-Point ii) Stability factor, S [8+7]

5.a) Compare CB, CE and CC amplifiers in view of A_V, A_I, R_I & R_O.
b) Estimate A_V, A_I, R_I & R_O in an Emitter Follower circuit with R_E = 1K, h_{ie} = 1100Ω, h_{fe} = 50, h_{re} = 2.4x 10^{-4}, h_{oe} = 25 μA/V. [7+8]

6.a) With neat sketches, necessary equations explain the drain & transfer characteristics of MOSFET in enhancement mode.
b) Why is a Field Effect Transistor called unipolar & voltage controlled device? Explain the drain & transfer characteristics of a JFET in detail. [7+8]

7.a) i) Give symbol of UJT and mark required polarities for operation.
ii) Explain how the UJT can be used as a negative-resistance device with the aid of static characteristics.
b) A Common Drain FET amplifier circuit shown in Figure.1 has the following circuit parameters: R_S = 0.5K, Rg = 1M, r_d = 5K, g_m= 5mS and V_{DD} = 20 V. Calculate A_V & R_O. [8+7]

JNTU WORLD

www.jntuworld.com

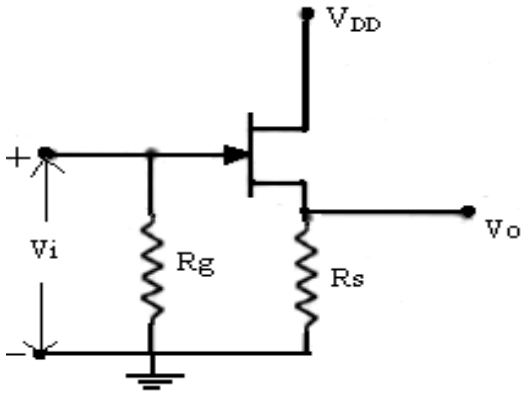

Figure.1

8.a) Draw the structure and two-transistor model of SCR, explain its operation with help of V-I characteristics.

b) Explain the operation of varactor diode with the help of neat diagrams. [10+5]

****

JNTUWORLD

www.jntuworld.com || www.android.jntuworld.com || www.jwjobs.net || www.android.jwjobs.net

R09

Code No: 09A30203

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B. Tech. II Year I Semester Examinations, May/June-2013
Electronic Devices and Circuits
(Common to EEE, ECE, CSE, EIE, BME, IT, MCT, ETM, ECOMPE, ICE)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

\- - -

1.a) Draw the V-I characteristics of a diode with zero cut-in voltage and equivalent resistance of 100 Ω. Draw the load line if R_L is also 100 Ω.
b) Draw the equivalent circuit of a diode circuit when a DC voltage to forward bias the diode along with an ac signal is applied.
c) Differentiate between normal PN junction diode and a Zener diode. [15]

2.a) Derive expressions for ripple factor, regulation and rectification efficiency of a half wave rectifier.
b) Design an LC filter for a Full wave rectifier to give 9V output as DC voltage at 100 mA current. Assume ripple factor to be 2%.
c) Compare the filtering characteristics of capacitance type, choke input type and Π-type filters. [15]

3.a) Based on the currents flowing through a BJT illustrate the amplification process.
b) Sketch the input and output characteristics of a BJT in CE configuration and discuss how β of the transistor can be determined form the characteristics.
c) Compare CB, CC, and CE configurations. [15]

4.a) What is the need of biasing a BJT for amplifier application? List the deficiencies of fixed bias and emitter feedback bias methods and explain how they are overcome in voltage divider bias method.
b) Define stability factors for a BJT with any biasing method. Suggest a method to compensate for temperature variation effects on operating point of a BJT circuit.
c) What is thermal runaway? Discuss the causes for it. [15]

5.a) Discuss the effect of V_{GS} on drain current of a JFET based on its structure.
b) Define: Pinch-off voltage, mutual conductance (g_m), dynamic drain resistance (r_d) and amplification factor (μ) for a JFET and establish a relation between them.
c) Explain the operation of a MOSFET in enhancement and depletion modes. [15]

6.a) What is the difference between approximate and accurate h-parameter models of a BJT in CE configuration? Discuss the conditions applicable for each model.
b) Draw the h-parameter equivalent circuit of a generalized BJT amplifier and derive expressions for A_v, A_i, R_i and R_o. [15]

7.a) Draw the circuit diagram, equivalent circuit of a JFET small signal amplifier in CS configuration and derive expressions for A_v, A_i, R_i and R_o. Make applicable assumptions and comments.

JNTUWORLD.COM

www.jntuworld.com || www.jwjobs.net

b) A 12 kΩ load resistance is connected to the output of a JFET CS amplifier. If R_G, R_S and C_S are given as 1MΩ, 1 kΩ and 25 μF respectively and μ, r_d of JFET are listed as 20 and 10 kΩ respectively, find the output voltage for a sinusoidal input of peak 0.1 volts at 2 kHz frequency. [15]

8.a) Which type of diode capacitance is utilized in varactor diode operation. Explain its principle of operation.

b) Name the device exhibiting negative resistance region in its V-I characteristic. With suitable diagram explain the operation of this device.

c) Discuss the constructional details of SCR and Schotky barrier diode. [15]

---oo0oo---

JNTUWORLD.COM

Code No: A109210203 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD

B.Tech II Year - I Semester Examinations, November/December, 2012

ELECTRONICS DEVICES AND CIRCUITS

(COMMON TO BME, CSE, EEE, ECE, E.COMP.E, EIE, ETM, IT, ICE, MCT)

Time: 3 hours **Max. Marks: 75**

Answer any five questions

All questions carry equal marks

---

1. a) Sketch V-I characteristics of a PN diode for the following conditions:

i) $R_f = 0$,	$V\gamma = 0$,	$R_r = \infty$
ii) $R_f = 0$,	$V\gamma = 0.6V$,	$R_r = \infty$
iii) R_f = Non-zero, fixed value,	$V\gamma = 0$,	$R_r = \infty$
iv) R_f = Non-zero, fixed value,	$V\gamma = 0.6V$,	$R_r = \infty$

Where $V\gamma$ is the cut-in voltage, R_f is the forward dynamic resistance & R_r is the reverse dynamic resistance of the diode.

b) Find the voltage drop across each of the silicon diodes shown in Figure.1 at room temperature. Assume that reverse saturation current flows in the circuit and the magnitude of the reverse breakdown voltage is greater than 5V?

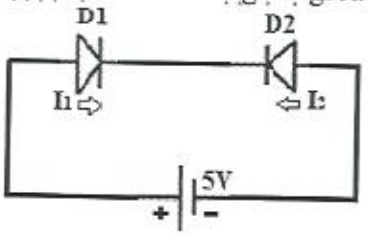

Figure.1

JNTU WORLD Hyderabad www.jntuworld.com

2.a) In a full-wave rectifier with capacitor filter, show that the ripple voltage is inversely proportional to the capacitance of the capacitor and is proportional to the load current. Calculate the ripple voltage, when C = 100μF and I_{DC} = 10mA. The ac input voltage to the rectifier is $V_m \sin 314t$.

b) Draw the circuit of Zener voltage regulator. Explain its operation with neat characteristics and also derive expressions for minimum and maximum values of source resistor for the Zener diode to work as a voltage regulator.

3.a) Explain Early effect and its consequences in a BJT. Also draw the Ebers-Moll model of a PNP transistor.

b) In the circuit shown in Figure.2, a silicon transistor with β =100, V_{BE}= 0.7V and V_{CEsat} = 0.2V is used. Determine whether the transistor is operated in active region or in saturation region?

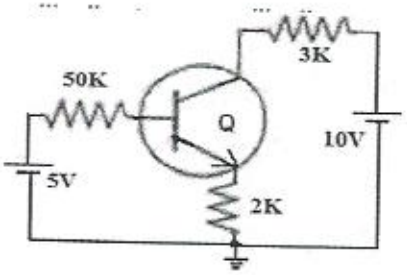

Figure:2

4. a) With neat diagram and necessary equations, explain how the variations in V_{BE} compensated with the variations in temperature.

b) Design a self bias circuit using silicon transistor to achieve a stability factor of 10, with the following specifications: $V_{CC} = 16V$, $V_{BE} = 0.7V$, $V_{CEQ} = 8V$, $I_{CQ} = 4$ mA and $\beta = 50$.

5. a) With neat diagrams and necessary equations, explain the effect of coupling capacitor and bypass capacitor on the performance of an amplifier at low-frequencies?

b) In a single stage CE amplifier circuit with unbypassed emitter resistor, $R_C = 10K$, $R_E = 1K$ and $R_S = 0.5K$. The h-parameters of the transistor used are $h_{ie} = 1.1K$, $h_{fe} = 50$, $h_{oe} = 25\ \mu A/V$ & $h_{re} = 2.5 \times 10^{-4}$. Find R_i and A_V.

6. a) Draw the basic structure and circuit arrangement of a P-channel Metal Oxide Semiconductor Field Effect Transistor in enhancement mode. Explain the drain and transfer characteristics.

b) Explain the procedure to obtain the small-signal equivalent circuit of a field effect transistor with necessary equations. Also draw the small-signal model.

7.a) What are the requirements of FET biasing? Verify these requirements in source self-bias circuit.

b) A Common Source FET amplifier circuit shown in Figure.3 with unbypassed R_S has the following circuit parameters: $R_d = 15K$, $R_S = 2.5K$, $Rg = 1M$, $r_d = 100K$, $I_{DSS} = 10mA$, $VP = -5V$and $V_{DD} = 20$ V. Calculate g_m & A_V. [7+8]

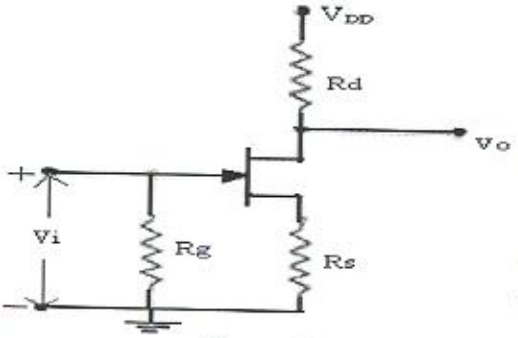

Figure.3

JNTU WORLD Hyderabad www.jntuworld.com

8.a) Draw the structure and two-transistor model of SCR, explain various methods of triggering an SCR.

b) With neat sketches, explain the principle of operation of Schottky Barrier Diode.

****

Code No: A109210203 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD

B.Tech II Year - I Semester Examinations, November/December, 2012

ELECTRONICS DEVICES AND CIRCUITS

(COMMON TO BME, CSE, EEE, ECE, E.COMP.E, EIE, ETM, IT, ICE, MCT)

Time: 3 hours **Max. Marks: 75**

Answer any five questions

All questions carry equal marks

---

1. a) Sketch V-I characteristics of a PN diode for the following conditions:

i) $R_f = 0$,	$V\gamma = 0$,	$R_r = \infty$
ii) $R_f = 0$,	$V\gamma = 0.6V$,	$R_r = \infty$
iii) R_f = Non-zero, fixed value,	$V\gamma = 0$,	$R_r = \infty$
iv) R_f = Non-zero, fixed value,	$V\gamma = 0.6V$,	$R_r = \infty$

Where $V\gamma$ is the cut-in voltage, R_f is the forward dynamic resistance & R_r is the reverse dynamic resistance of the diode.

b) Find the voltage drop across each of the silicon diodes shown in Figure.1 at room temperature. Assume that reverse saturation current flows in the circuit and the magnitude of the reverse breakdown voltage is greater than 5V?

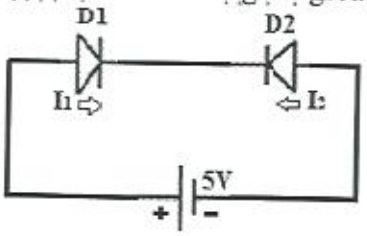

Figure.1

JNTU WORLD Hyderabad www.jntuworld.com

2.a) In a full-wave rectifier with capacitor filter, show that the ripple voltage is inversely proportional to the capacitance of the capacitor and is proportional to the load current. Calculate the ripple voltage, when C = 100μF and I_{DC} = 10mA. The ac input voltage to the rectifier is $V_m \sin 314t$.

b) Draw the circuit of Zener voltage regulator. Explain its operation with neat characteristics and also derive expressions for minimum and maximum values of source resistor for the Zener diode to work as a voltage regulator.

3.a) Explain Early effect and its consequences in a BJT. Also draw the Ebers-Moll model of a PNP transistor.

b) In the circuit shown in Figure.2, a silicon transistor with β =100, V_{BE}= 0.7V and V_{CEsat} = 0.2V is used. Determine whether the transistor is operated in active region or in saturation region?

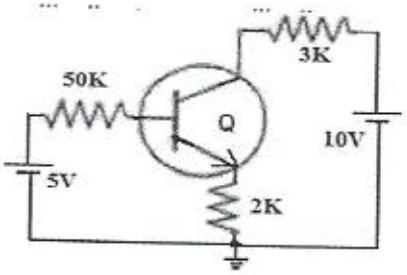

Figure:2

4. a) With neat diagram and necessary equations, explain how the variations in V_{BE} compensated with the variations in temperature.

b) Design a self bias circuit using silicon transistor to achieve a stability factor of 10, with the following specifications: $V_{CC} = 16V$, $V_{BE} = 0.7V$, $V_{CEQ} = 8V$, $I_{CQ} = 4$ mA and $\beta = 50$.

5. a) With neat diagrams and necessary equations, explain the effect of coupling capacitor and bypass capacitor on the performance of an amplifier at low-frequencies?

b) In a single stage CE amplifier circuit with unbypassed emitter resistor, $R_C = 10K$, $R_E = 1K$ and $R_S = 0.5K$. The h-parameters of the transistor used are $h_{ie} = 1.1K$, $h_{fe} = 50$, $h_{oe} = 25\ \mu A/V$ & $h_{re} = 2.5 \times 10^{-4}$. Find R_i and A_V.

6. a) Draw the basic structure and circuit arrangement of a P-channel Metal Oxide Semiconductor Field Effect Transistor in enhancement mode. Explain the drain and transfer characteristics.

b) Explain the procedure to obtain the small-signal equivalent circuit of a field effect transistor with necessary equations. Also draw the small-signal model.

7.a) What are the requirements of FET biasing? Verify these requirements in source self-bias circuit.

b) A Common Source FET amplifier circuit shown in Figure.3 with unbypassed R_S has the following circuit parameters: $R_d = 15K$, $R_S = 2.5K$, $Rg = 1M$, $r_d = 100K$, $I_{DSS} = 10mA$, $VP = -5V$and $V_{DD} = 20$ V. Calculate g_m & A_V. [7+8]

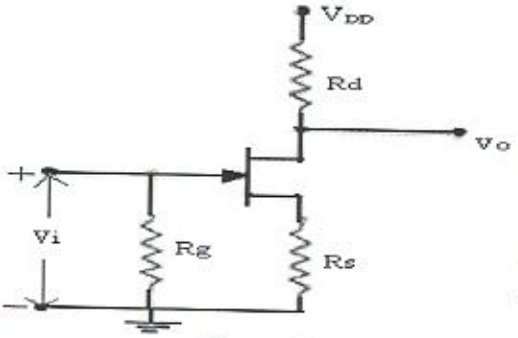

Figure.3

JNTU WORLD Hyderabad www.jntuworld.com

8.a) Draw the structure and two-transistor model of SCR, explain various methods of triggering an SCR.

b) With neat sketches, explain the principle of operation of Schottky Barrier Diode.

****

www.jntuworld.com www.jwjobs.net

Code No:A109210203 | R09 | SET-1

B.Tech II Year I Semester Examinations, May-June, 2012
ELECTRONIC DEVICES AND CIRCUITS
(COMMON TO BME, CSE, EEE, ECE, ECC, EIE, ETM, IT, ICE, MCT)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

\- - -

1.a) Explain the concept of diode capacitance. Derive expression for transition capacitance?
b) Find the value of D.C. resistance and A.C resistance of a Germanium junction diode at 25^0 C with reverse saturation current, I_o = 25μA and at an applied voltage of 0.2V across the diode. [8+7]

2. Define the following terms and derive the equations with respect to half-wave rectifier:
i) Ripple factor ii) Peak inverse voltage
iii) Rectification efficiency iv) % Regulation. [15]

3.a) With neat sketches and necessary waveforms, explain the input and output characteristics of a BJT in CB configuration. Also derive expression for output current.
b) Derive the relation among α, β and γ. [10+5]

4.a) Explain the basic requirements of transistor biasing. Verify these requirements in collector to base bias circuit.
b) Design a fixed bias circuit using silicon transistor, with the following specifications: V_{CC} = 16V, V_{BE} = 0.7V, V_{CEQ} = 8V, I_{CQ} = 4 mA & β= 50. [8+7]

5. Draw the circuit diagram, AC equivalent & small signal equivalent of Common Base amplifier using accurate h-parameter model. Derive expressions for A_{Vs}, A_{Is}, R_I & R_O. [15]

6.a) Explain the construction & operation of an N-channel enhancement and depletion MOSFET with the help of static drain characteristics and transfer characteristics.
b) Define pinch-off voltage and transconductance in field effect transistors. [12+3]

7.a) Draw the small-signal model of common drain FET amplifier. Derive expressions for voltage gain and output resistance.
b) Calculate voltage gain $A_V = V_O/V_i$ and R_O at 1KHz for the circuit shown in Figure.1. FET parameters are gm=2mA/V and rd =10k. Neglect capacitances. [8+7]

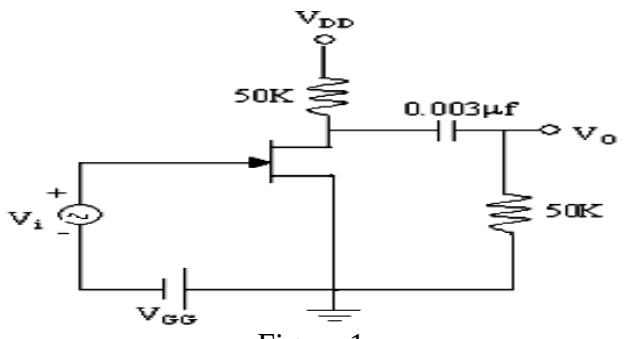

Figure.1

8. With neat energy band diagrams, explain the V-I characteristics of Tunnel diode in detail. Also explain the negative-resistance region in the characteristics and applications of Tunnel diode. [15]

****

www.jntuworld.com

www.jntuworld.com www.jwjobs.net

Code No:A109210203 | R09 | SET-2

B.Tech II Year - I Semester Examinations, May-June, 2012
ELECTRONIC DEVICES AND CIRCUITS
(COMMON TO BME, CSE, EEE, ECE, ECC, EIE, ETM, IT, ICE, MCT)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

\- - -

1.a) What do you understand by depletion region at p-n junction? What is the effect of forward and reverse biasing of p-n junction on the depletion region? Explain with necessary diagrams.
b) Explain Zener and avalanche breakdown mechanisms in detail. [8+7]

2.a) Draw the circuit diagram of full-wave rectifier with inductor filter. Explain its operation with necessary equations.
b) A HWR circuit supplies 100mA DC current to a 250Ω load. Find the DC output voltage, PIV rating of a diode and the r.m.s. voltage for the transformer supplying the rectifier. [8+7]

3.a) With neat sketches and necessary waveforms, explain the input and output characteristics of a BJT in CE configuration. Also derive expression for output current.
b) Calculate the collector current and emitter current for a transistor with $\alpha = 0.99$ and $I_{CBO} = 50\mu A$ when the base current is $20\mu A$. [10+5]

4.a) What is thermal runaway in transistors? Obtain the condition for thermal stability in transistors.
b) Design a self bias circuit using silicon transistor to achieve a stability factor of 10, with the following specifications: $V_{CC} = 16V$, $V_{BE} = 0.7V$, $V_{CEQ} = 8V$, $I_{CQ} = 4$ mA & $\beta = 50$. [6+9]

5. Draw the circuit diagram, AC equivalent & small signal equivalent of Emitter Follower amplifier using accurate h-parameter model. Derive expressions for A_{Vs}, A_{Is}, R_I & R_O. [15]

6.a) With the help of neat sketches and characteristic curves explain the construction & operation of a JFET and mark the regions of operation on the characteristics.
b) Derive expression for transconductance in a field effect transistor. [10+5]

7.a) Draw the small-signal model of common source FET amplifier. Derive expressions for voltage gain and output resistance.
b) Give the UJT symbol and simplified equivalent circuit with external resistors included. Describe its negative-resistance nature, with the help of V-I characteristics. [7+8]

8.a) With neat sketches, explain the principle of operation of Schottky Barrier Diode.
b) With neat sketches, explain V-I characteristics of semiconductor Photo Diode. [8+7]

****

JNTUWORLD

www.jntuworld.com

www.jntuworld.com www.jwjobs.net

Code No:A109210203 | R09 | SET-3

B.Tech II Year - I Semester Examinations, May-June, 2012
ELECTRONIC DEVICES AND CIRCUITS
(COMMON TO BME, CSE, EEE, ECE, ECC, EIE, ETM, IT, ICE, MCT)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

\- - -

1.a) Explain about various current components in a forward biased p-n junction diode.
b) With neat sketches and necessary waveforms explain about the regulation characteristics of Zener diode. [7+8]

2.a) Draw the circuit of full-wave rectifier with capacitor filter. Explain its operation with necessary equations.
b) A full wave rectifier circuit uses two silicon diodes with a forward resistance of 20Ω each. A DC voltmeter connected across the load of 1KΩ reads 55.4 volts. Calculate
i) I_{rms} ii) Average voltage across each diode
iii) ripple factor iv) Transformer secondary voltage rating. [7+8]

3.a) With neat sketches and necessary waveforms, explain the input and output characteristics of a BJT in CE configuration. Also derive expression for output current.
b) The reverse leakage current of the transistor when connected in CB configuration is 0.2 μA while it is 18 μA when the same transistor is connected in CE configuration. Calculate α and β of the transistor. [10+5]

4.a) Explain how I_{CO} variations are compensated with the help of diode and thermistor in transistor biasing circuits?
b) Design a collector to base bias circuit using silicon transistor to achieve a stability factor of 20, with the following specifications: V_{CC} = 16V, V_{BE} = 0.7V, V_{CEQ} = 8V, I_{CQ} = 4 mA & β= 50. [7+8]

5. Draw the basic circuit, ac equivalent and h-parameter model of a Common Emitter amplifier. Derive expressions for A_{Vs}, A_{Is}, R_I & R_O. [15]

6.a) Explain the construction & operation of an P-channel enhancement and depletion MOSFET with the help of static drain characteristics and transfer characteristics.
b) Explain why field effect transistor is called as unipolar and voltage controlled device. [12+3]

7.a) Draw the small-signal model of common gate FET amplifier. Derive expressions for voltage gain and input resistance.
b) A Common Source FET amplifier circuit shown in Figure.1 with unbypassed R_S has the following circuit parameters: R_d = 15K, R_S = 0.5K, Rg = 1M, r_d = 5K, g_m= 5mS and V_{DD} = 20 V. Calculate A_V & R_O. [8+7]

JNTUWORLD

www.jntuworld.com

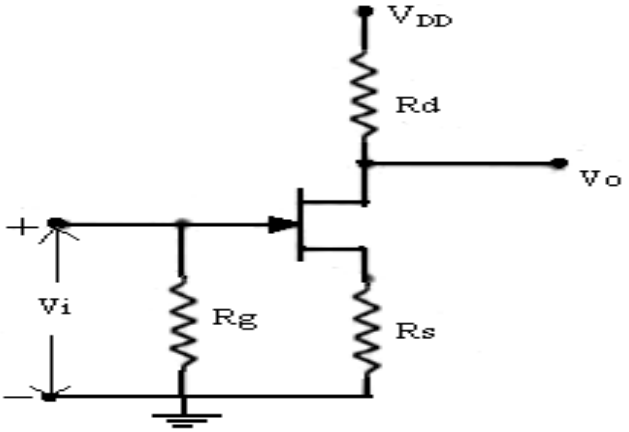

Figure.1

8. With neat energy band diagrams, explain the V-I characteristics of Tunnel diode in detail. Also explain the negative-resistance region in the characteristics. [15]

****

JNTUWORLD

www.jntuworld.com www.jwjobs.net

Code No:A109210203 | R09 | SET-4

B.Tech II Year - I Semester Examinations, May-June, 2012
ELECTRONIC DEVICES AND CIRCUITS
(COMMON TO BME, CSE, EEE, ECE, ECC, EIE, ETM, IT, ICE, MCT)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

- - -

1.a) With neat sketches and necessary waveforms explain the volt ampere characteristics of PN diode.
b) Explain the temperature dependence of VI characteristics of PN diode.
c) Compare ideal and practical diodes. [8+4+3]

2.a) Draw the circuit of full-wave rectifier with L-section filter and derive expression for its ripple factor.
b) A 230 V, 60Hz voltage is applied to the primary of a 5:1 step down, center tapped transformer used in a full wave rectifier having a load of 900Ω .If the diode resistance and the secondary coil resistance together has a resistance of 100Ω, determine
i) dc voltage across the load. ii) dc current flowing through the load.
iii) dc power delivered to the load. iv) PIV across each diode. [7+8]

3.a) With the help of a neat diagram explain different current components in an NPN bipolar junction transistor.
b) With reference to bipolar junction transistors, define the following terms and explain.
i) Emitter efficiency.
ii) Base Transportation factor.
iii) Large signal current gain. [9+6]

4.a) Explain the basic requirements of transistor biasing. Verify these requirements in Emitter feedback bias circuit.
b) An NPN Silicon transistor with β=50 is used in a common emitter circuit with V_{CC}=10V, R_C=2K. The bias is obtained by connecting a 100K resistance from collector to base. Find
i) Q-Point ii) Stability factor, S [8+7]

5.a) Compare CB, CE and CC amplifiers in view of A_V, A_I, R_I & R_O.
b) Estimate A_V, A_I, R_I & R_O in an Emitter Follower circuit with R_E = 1K, h_{ie} = 1100Ω, h_{fe} = 50, h_{re} = 2.4x 10^{-4}, h_{oe} = 25 μA/V. [7+8]

6.a) With neat sketches, necessary equations explain the drain & transfer characteristics of MOSFET in enhancement mode.
b) Why is a Field Effect Transistor called unipolar & voltage controlled device? Explain the drain & transfer characteristics of a JFET in detail. [7+8]

7.a) i) Give symbol of UJT and mark required polarities for operation.
ii) Explain how the UJT can be used as a negative-resistance device with the aid of static characteristics.
b) A Common Drain FET amplifier circuit shown in Figure.1 has the following circuit parameters: R_S = 0.5K, Rg = 1M, r_d = 5K, g_m= 5mS and V_{DD} = 20 V. Calculate A_V & R_O. [8+7]

JNTU WORLD

www.jntuworld.com

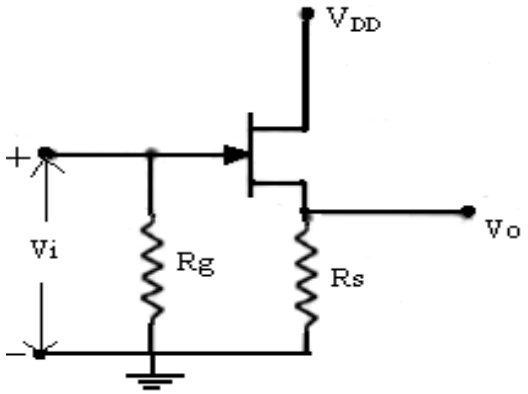

Figure.1

8.a) Draw the structure and two-transistor model of SCR, explain its operation with help of V-I characteristics.

b) Explain the operation of varactor diode with the help of neat diagrams. [10+5]

****

JNTUWORLD